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EXAMINER	
GOSSAGE, GLENN A	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,960	WILCOX ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 March 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN A MEMORY BY SELECTIVELY DISABLING AND ENABLING SENSE AMPLIFIERS-- is suggested (see claims 1, 8, 15 and 21, lines 1 and 4, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

2. The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). It appears in line 1, "technique" should be changed to --method and apparatus for selectively disabling sense amplifiers in order to reduce power consumption in a computer system are disclosed. The method-- or other similar language for clarity and completeness (see claims 1 and 15, lines 1 and 4, and claim 27, lines 1 and 8, e.g.).

Also, one or two sentences should be added describing additionally claimed and disclosed features. [For example, in line 5, after "bus.", insert sentences such as --The disabling of the amplification may be synchronized to an edge of a delayed data strobe signal (DQS). Signals associated with a double data rate (DDR) synchronous dynamic random access memory (SDRAM) memory device may be communicated over the memory bus--. See claims 4-5 and 11-12, as well as page 1, line 10 to page 2, line 23, e.g. Also, in line 3, after "absence," insert --or end-- (note claims 3 and 16, e.g.).]

Appropriate correction is required. See MPEP § 608.01(b).

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on March 5, 2002 have been disapproved by the examiner for the reasons below.

The drawings are objected to because in Figure 1, within "box" 16, it appears "MEMORY HUB" should be --MEMORY CONTROLLER HUB-- for clarity and consistency (see page 3, lines 16-17, 19 and 23, e.g.).

In Figure 3, it appears the reference numeral 100 (for the "box" shown in dashed lines?) is missing (see page 6, line 27 and page 7, line 23, e.g.). Similarly, it appears the reference numeral 106 (for the DQS line?) is missing (see page 7 lines 24-25). The reference numeral 124 (on the output line/bus of write path circuitry 120?) is also apparently missing (see page 7, line 26). Within "box" 108, it appears "DLY" should be --DELAY-- for clarity. Additionally, within "box" 102, it appears "AMP" should be --AMPS-- for consistency (see page 7, line 8 and claim 15, line 2, e.g.). Also, the line between the output of the write path circuitry and the DQS line is confusing (the DQ line/bus 104 appears to be connected to the DQS line). [Should the line be deleted, and a DQS input added to "box" 120? See, for example, the EOB input shown to "box" 114, which is sent on the line/bus output from the control circuit 142.] Moreover, it appears the sense amp control circuit 114 should be shown as receiving (the inverse of) the delayed DQS signal (output from delay circuit 108) for consistency (see Fig. 11). [Should "DQS" be

p 8, l 4-5, l 14-16, 24

relabeled --DQS DELAYED # --, and the input to circuit 108 be "separated" from this input and relabeled --DQS--?]

In Figures 4-10, the symbol "Z" within the waveforms is somewhat confusing. It appears the symbols should simply be deleted for clarity.

In Figure 11, it appears the SCLK input to the read buffer latches 151 and 150 should be shown for clarity and consistency (see Figure 3, e.g.).

In Figure 12, it appears a label such as --DATA I/F-- should be inserted within "box" 100 for clarity.

Applicant is REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) (submission of corrected formal drawings, e.g.) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

4. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, line 3, it appears "The" reads more clearly here as --This-- or --The present--.

On page 3, line 3, the wording "Fig. 11 (shows) control circuitry for a sense amplifier" is somewhat confusing when read in conjunction with Fig. 11. It appears "control circuitry for" should be changed to --read buffer circuitry and control circuitry coupled to-- for clarity and consistency with Fig. 11. In line 11, it appears "10" should be moved after "system" for clarity and consistency (see lines 13 and 20, e.g.).

On page 6, line 21, it appears --over hub link 34-- should be inserted after "system" for clarity and completeness (see Fig. 2, and also note page 10, line 15). Also in line 21, and throughout the specification, the first occurrence of all acronyms or abbreviations should be written out for clarity, whether or not they may be considered "well known." Accordingly, "I/O" should be written out as --input/output (I/O)--. See also page 10, lines 21 and 22.

On page 7, line 7, it appears "a" should be deleted. In line 27, it appears --read-- should be inserted before "data" for consistency (see Fig. 3 and lines 30-31).

On page 8, line 22, the wording "As depicted in Fig. 9, the flip-flop 154" is somewhat confusing. It appears "As depicted in Fig. 9, the" should be changed to --The--, and -- , depicted in Fig. 9, -- inserted after "EOB signal" for clarity. In line 24, it appears "delay" should be --delayed-- for consistency (note lines 5 and 27-28).

On page 9, line 1, it appears --(Fig. 3)-- should be inserted after "142" for clarity. In line 25, it appears "input" (first occurrence) should be --output-- for clarity and consistency (see Fig. Also in line 25, as well as line 28, it appears "buffer 152" should be --inverter 152-- for

clarity and consistency (see page 8, line 24 and Fig. 11). In line 30, it appears --are-- should be inserted before "within" for clarity (so that the sentence is complete).

On page 10, line 28, "this" appears to read more clearly here as --the--.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 1, line 2, it appears --received-- should be inserted before "from" for consistency (see claim 15, line 2, e.g.).

In claims 2 and 3, line 1, it appears --the amplification-- should be inserted after "disabling" for consistency (see claim 1, line 4, e.g.).

In claim 4, line 4, it appears "disablement" should be --disabling-- for consistency (see claim 1, line 4, e.g.).

In claim 8, line 2, it appears --received-- should be inserted before "from" for consistency, analogous to claim 1 (see claim 21, line 2, e.g.).

In claims 9 and 10, line 1, it appears --the amplification-- should be inserted after "enabling" for consistency (see claim 8, line 4, e.g.).

In claim 11, line 4, it appears "enablement" should be changed to --enabling of the

[illegible]cation-- for consistency (see claim 8, line 4, as well as claim 4, line 4, e.g.).

Appropriate correction is required.

5. Claims 8-14, 21-26 and 29-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 8, and therefore its dependent claims, it is not entirely clear how the amplifiers are enabled "in response to a predetermined operation occurring." It appears --the beginning of-- should be inserted after "to" in line 4 for clarity and consistency (see page 5, lines 22-23; page 6, lines 1-4; page 7, lines 12-13; and page 9, line 9, e.g.). [Note that it appears claim 10 should then be canceled. In this regard, also see 35 U.S.C. 112, fourth paragraph, as well as 37 CFR 1.75(b) and (c).]

In claim 21, and therefore its dependent claims, the proper antecedent for "the predetermined operation" is not clear. It is also not entirely clear how the amplifiers are enabled "in response to the predetermined operation occurring." It appears --beginning of a-- should be inserted after "to the" in line 4 for clarity and consistency (again see page 5, lines 22-23; page 6, lines 1-4; page 7, lines 12-13; and page 9, line 9, e.g.).

In claim 29, lines 8-9, the proper antecedent for "the predetermined operation" is not clear. It is also not entirely clear how the amplifiers are enabled "in response to the predetermined operation occurring" analogous to claim 21. It appears "predefined" in line 4 should be changed to --predetermined--, and --beginning of the-- inserted after "to the" in line 8 for clarity and

consistency (again see page 5, lines 22-23; page 6, lines 1-4; page 7, lines 12-13; and page 9, line 9, as well as claim 27, line 4, e.g.).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-3, 6, 15-17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

The claims as broadly construed and interpreted, particularly with regard to the memory "bus," "read on" a method and apparatus disclosed by Huang et al, and thus the invention as broadly set forth in the claims is seen to be anticipated by Huang et al. [In this regard, also see MPEP 706.02(m) regarding form paragraph 7.27, Examiner Note 1a, and also see numbered paragraph 8 below.]

With respect to claim 1, as well as claim 15, Huang et al discloses a method and apparatus for controlling amplification in a memory of a computer system so as to reduce power consumption. Huang et al discloses providing amplifiers for amplifying data signals from a memory bus [Huang et al teaches that data signals on complementary pairs of bit lines, which represent bits of data output from an SDRAM, may be amplified by sense amplifiers. See column 3, lines 13-27 and Figure 1, e.g.], and providing a "first circuit" for "sampling" the amplified data signals [the amplified data signals may be "sampled" by a pair of latch circuits 22, 32 and an output buffer 24, e.g.]. Huang et al further teaches providing ("second") circuitry for selectively disabling the amplification in response to the absence of a predetermined operation occurring over the memory bus [Huang et al teaches selectively disabling the sense amplifiers when a predetermined operation such as a read operation is complete, i.e. "in the absence of" a predetermined operation such as a read operation. See column 1, lines 46-51; column 2, lines 39-54; column 5, line 48 to column 6, line 24, e.g.].

With respect to claims 2-3 and 6, as well as claims 16-17, Huang et al teaches that the "selectively disabling" comprises selectively disabling sense amplifiers, and that the selectively disabling is performed in response to the end or completion of a particular predetermined operation such as a read data output operation (again see column 1, lines 46-51 and column 6, lines 17-24).

With respect to claim 19, the apparatus of Huang et al includes circuitry for controlling various components of a memory and thus the "apparatus" of Huang et al may be broadly considered to be a memory "controller."

With respect to claim 20, Huang et al teaches that the apparatus may comprise a memory device such as an SDRAM device.

7. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Taruishi et al (U.S. Patent 6,339,552).

The claims "read on" a method and apparatus disclosed by Taruishi et al, and thus the invention as broadly set forth in the claims is seen to be anticipated by Taruishi et al.

More specifically, with respect to claims 1 and 8, as well as claims 15 and 21, and claims 27 and 29, Taruishi et al (U.S. 6,339,552) discloses a method and apparatus for controlling amplification in a memory of a computer system so as to reduce power consumption, as in the claimed invention. Taruishi et al discloses providing amplifiers for amplifying data signals from a memory bus [Taruishi et al discloses that sense amplifiers within data I/O circuits (DIO0-DIO3) in Figure 1 are used to amplify data signals from a memory "bus" in a well known manner. See column 5, lines 59-64, e.g.] and providing a "first circuit" for "sampling" the amplified data signals [a data output circuit 4 in Figure 1 may be used to "sample" the amplified data signals, e.g.]. Taruishi et al further teaches providing ("second") circuitry for selectively enabling and disabling the amplification in response to whether a predetermined operation occurs

over a memory bus [Taruishi et al teaches selectively enabling the sense amplifiers in response to a "predetermined" operation occurring over a memory bus in a particular bank and selectively disabling the sense amplifiers when a predetermined operation is not occurring over a memory bus in a particular bank. See column 6, lines 33-40, e.g.]. Attention is also respectfully directed to column 2, lines 24-41 and 57-62; column 4, lines 39-51; and column 12, lines 1-16.

[Note that reference is made to U.S. Patent 6,339,552 (which is an English language patent family member of JP 2001-067877) for convenience.]

Also with respect to claims 27 and 29, Taruishi et al discloses that the memory may be utilized in a computer system such as a microcomputer which, as one of ordinary skill in the art would recognize, includes some sort of processor which initiates a predetermined operation with the memory using a clock signal and the various "commands" or instructions discussed throughout Taruishi et al (see column 17, lines 45-47, as well as column 8, lines 16+, e.g.).

With respect to claims 2 and 9, Taruishi et al teaches that the "selectively disabling" comprises selectively disabling sense amplifiers (again see column 6, lines 33-40, e.g.).

With respect to claims 3 and 10, as well as claims 16 and 22, Taruishi et al teaches that the "selectively disabling" and "selectively enabling" comprises selectively enabling sense amplifiers as discussed above (again see column 6, lines 33-40). The selective enabling and disabling of the sense amplifiers in Taruishi et al may be considered to occur in response to the beginning and end of a "predetermined" operation such as when a particular bank is selected/deselected for a read or write operation, i.e the enabling of the sense amplifiers is performed in response to the

beginning of a read/write operation when a bank is selected for operation and the disabling of the sense amplifiers is performed in response to the end or completion of a particular predetermined operation such as a read or write operation when a bank is deselected.

With respect to claim 4, Taruishi et al teaches reading a data strobe signal (DQS) which controls reading and writing operations in an SDRAM memory in a well known manner, and also teaches delaying the data strobe signal. Taruishi et al further teaches that data input and output operations may be synchronized to the edge of a data strobe signal that appears on a memory bus in connection with the predetermined operation or a delayed data strobe signal so as to provide reliable data input and output operations (see column 7, lines 32-59, e.g.).

With respect to claims 5 and 12, Taruishi et al also teaches "communicating" signals associated with a double data rate (DDR) synchronous dynamic random access memory (SDRAM) device over the memory bus (see column 1, lines 5-10 and column 5, lines 13-15, e.g.).

With respect to claims 6 and 7, as well as claims 13-14, 17-18, 23-24, 28 and 30, one of ordinary skill in the art would readily appreciate that the operation for which a particular bank may be selected in Taruishi et al may be a read or write operation.

With respect to claim 11, Taruishi et al teaches that data input and output and input operations may be synchronized to the edge of a data strobe signal that appears on a memory bus in connection with the predetermined operation (again see column 7, lines 32-59, e.g.).

With respect to claims 19 and 25, the apparatus of Taruishi et al includes circuitry for controlling various components of a memory and thus the "apparatus" of Taruishi et al may be broadly considered to be a memory "controller."

With respect to claims 20 and 26, Taruishi et al teaches that the apparatus may comprise a memory device such as an SDRAM device as discussed above (again see column 1, lines 5-10 and column 5, lines 13-15, e.g.).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 4 to page 2, line 8 of the specification, e.g.) in view of Huang et al.

With respect to claim 1, as well as claims 15 and 27, applicants' admitted prior art discloses a method and apparatus for controlling operations in a memory such as a synchronous dynamic random access memory (SDRAM), the method including amplifying data signals from a memory bus using sense amplifiers and "sampling" the amplified data signals (see page 1, line 4 to page 2, line 8 of the specification, e.g.), but does not teach selectively disabling the amplification by

the (sense) amplifiers in response to the "absence" of a predetermined operation in order to reduce power consumption.

Huang et al similar discloses a method and apparatus for controlling operations in a memory including amplifying data signals in a memory, and teaches selectively disabling the sense amplifiers in response to the "absence" of a predetermined operation in order to reduce power consumption (see column 1, lines 46-51; column 2, lines 39-54; column 5, line 48 to column 6, line 24, e.g.). Huang et al also specifically teaches selectively disabling sense amplifiers in a synchronous dynamic random access memory (SDRAM).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to selectively disable the sense amplifiers in the SDRAM of applicants' admitted prior art in response to the "absence" of a predetermined operation because Huang et al teaches that a reduced power consumption may be obtained in such an SDRAM, a highly desirable feature in a memory device operating with a high frequency clock signal such as an SDRAM.

With respect to claim 8, as well as claims 21 and 29, and claim 9, Huang et al teaches selectively disabling the sense amplifiers in response to the "absence" of a predetermined operation, and thus one of ordinary skill in the art would have found it obvious to enable the sense amplifiers during the "presence" of a predetermined operation on the bus.

Also with respect to claims 27 and 29, applicants' admitted prior art discloses that SDRAMs may be utilized in computer systems which include a memory controller and, as one of ordinary

skill in the art would appreciate, a processor which initiates a predetermined operation with the memory using a clock signal and various "commands" or instructions.

With respect to claims 2-3 and 6, as well as claims 13, 16-17, 22-23, 28 and 30, Huang et al teaches that the "selectively disabling" comprises selectively disabling sense amplifiers, and that the selectively disabling is performed in response to the end or completion of a particular predetermined operation such as a read data output operation (again see column 1, lines 46-51 and column 6, lines 17-24).

With respect to claim 5, as well as claims 12, 20 and 26, applicants' admitted prior art teaches that the apparatus may comprise a memory device such as a double data rate (DDR) SDRAM device (see page 1, lines 10-23 and page 2, lines 5-8 of the present specification).

With respect to claim 7, as well as claims 14, 18 and 24 (and claims 28 and 30), while Huang et al only specifically teaches selectively disabling the sense amplifiers in an SDRAM for a read operation, one of ordinary skill in the art at the time the claimed invention was made provided with this teaching would have found it readily obvious to also selectively disable the sense amplifiers in the SDRAM of applicants' admitted prior art for a write operation so as to further decrease or reduce the amount of power consumption in the computer system.

With respect to claim 10, Huang et al teaches selectively disabling the sense amplifiers in response to the "absence" of a predetermined operation, and thus one of ordinary skill in the art would have found it obvious to enable the sense amplifiers during the presence of a predetermined operation, as discussed above with respect to claim 8. Thus, it would have been

obvious to enable the sense amplifiers at the beginning, or during the presence, of a predetermined operation, and then to disable the sense amplifiers during the absence, or at the end or completion, of the predetermined operation, in order to maximize power savings.

With respect to claim 11, applicants' admitted prior art discloses that signals are communicated to and from the SDRAM device in synchronization with the edges of a data strobe signal that appears on a memory bus (see page 1, lines 10-13 of the present specification) and thus it would have been obvious to synchronize a sense amplifier enable/disable signal in order to reliably amplify the data signals at the appropriate timing.

With respect to claims 19 and 25, applicants' admitted prior art discloses that the "apparatus" may be a memory controller (see page 1, lines 6-9 and page 2, lines 1-4 of the present specification).

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 4 to page 2, line 8 of the specification, e.g.) in view of Huang et al as applied to claims 1-3 and 5-30 above (see numbered paragraph 8), and further in view of Yanagawa.

With respect to claim 4, applicants' admitted prior art in view of Huang et al discloses a method and apparatus for controlling operations in a memory such as a synchronous dynamic random access memory (SDRAM) including amplifying data signals from a memory bus using sense amplifiers, "sampling" the amplified data signals, and selectively disabling the

amplification by the (sense) amplifiers in response to the "absence" of a predetermined operation in order to reduce power consumption (see numbered paragraph 8 above, e.g.). Applicants' admitted prior art also teaches that data signals are communicated to and from the SDRAM device in synchronization with the edges of a data strobe signal that appears on a memory bus (see page 1, lines 10-13 of the present specification), but does not teach delaying the data strobe signal and synchronizing communication of the signals to and from the SDRAM device in synchronization with an edge of the delayed data strobe signal.

Yanagawa similarly discloses a SDRAM device in which signals are communicated to and from the SDRAM device in synchronization with the edges of a data strobe signal in a well known manner, and additionally teaches delaying the data strobe signal and synchronizing communication of the signals to and from the SDRAM device in synchronization with an edge of the delayed data strobe signal in order to reliably control the input and output of data from the memory device (see paragraphs [0004] - [0005] and [0010] - [0012], e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to delay a data strobe signal and synchronize communication of the signals to and from an SDRAM device in synchronization with an edge of the delayed data strobe signal, as taught by Yanagawa, in the SDRAM device of applicants' admitted prior art in view of Huang et al as previously discussed, in order to reliably control the input and output of data from the memory device.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wang et al is cited as disclosing a method and apparatus for selectively disabling and enabling sense amplifiers in a memory device in order to reduce power consumption similar to the present invention (see column 1, lines 10-27 and 41-53; column 2, lines 46-67; and column 3, lines 19-29, e.g.).

Matsubara is cited as disclosing a synchronous dynamic random access memory with reduced power consumption similar to the present invention.

Jeddeloh (U.S. '612), Jeddeloh (U.S. '213) and Vogt et al are cited as disclosing providing a delayed data strobe or clock signal in order to optimize read and write timing and reliably control the input and output of data similar to the present invention.

Applicants and applicants' attorneys are also respectfully reminded of the duty to disclose under 37 CFR 1.56 any information which may be material to the examiner in deciding whether to allow the claims of the present application. More specifically, any information regarding the SDR and DDR SDRAM devices and computer systems described on pages 1-2 in the background section of the present specification or other similar devices, as well as devices or memory (controller) hubs from Intel Corporation, the assignee of the present invention, should be submitted for proper consideration by the examiner.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187